CLAIMS

We claim:

1. A method of manufacturing a semiconductor device, comprising:

forming a trench dielectric that has a sidewall adjacent to the active area of the substrate;

forming a spacer over the sidewall, the spacer covering the sidewall at least at a bottom portion, near the active area;

exposing the dielectric and spacer to an etchant, with the spacer protecting at least the bottom portion of the sidewall; and

removing the spacer.

2. The method of Claim 1, wherein the spacer is formed of an anti-reflective coating (ARC).

3. The method of Claim 2, wherein the spacer is formed of an ARC comprising propylene glycol monomethyl ether, aromatic sulfur compound, acrylic polymer, non-ionic surfactant, residual acrylate monomer, amidomethyl ether crosslinker, and 2-methoxy-1-propanol.

4. The method of Claim 2, wherein the spacer is formed of silicon nitride or silicon oxynitride.

5. The method of Claim 1, wherein the spacer has a width at the bottom between about 400 Å and about 1,000 Å.

6. The method of Claim 1, wherein the spacer is removed by ashing in an oxygen environment.

7. The method of Claim 1, wherein the spacer is removed by a liquid strip process using phosphoric acid.

8. A method of manufacturing a semiconductor device, comprising:

providing a substrate having a substantially planar surface;

providing a first oxide layer over the substrate;

providing a trench in the substrate through the first oxide layer, an intersection of the trench and the surface of the substrate forming a corner;

providing a dielectric layer that fills the trench to a level above the first oxide layer;

forming a spacer aligned with the dielectric layer;

etching a portion of the first oxide layer around the spacer, the spacer protecting the dielectric layer from loss proximate the corner; and

providing a second oxide layer over the substrate between remaining portions of the first oxide layer, the second oxide layer having a smaller thickness than the remaining portions of the first oxide layer.

9. The method of Claim 8, wherein the first oxide layer is different from the second oxide layer.

10. The method of Claim 9, wherein the first oxide layer is aluminum oxide and the second oxide layer is silicon dioxide.

11. The method of Claim 8, wherein the spacer is removed after etching the portion of the first oxide layer.

12. A method of manufacturing a semiconductor device, comprising:

providing a substrate having a substantially planar surface;

providing a first oxide layer over the substrate;

providing a trench in the substrate through the first oxide layer, an intersection of the trench and the surface of the substrate forming a corner;

providing a dielectric layer that fills the trench to a level above the first oxide layer;

forming a spacer aligned with the dielectric layer;

etching a portion of the first oxide layer around the spacer, the spacer protecting the dielectric layer from loss proximate the corner; and

providing a second oxide layer over the substrate between remaining portions of the first oxide layer, the second oxide layer having a lower capacitance per unit area than the remaining portions of the first oxide layer.

13. The method of Claim 12, wherein the first oxide layer is different from the second oxide layer.

14. The method of Claim 12, wherein the spacer is removed after etching the portion of the first oxide layer.

15. A method of manufacturing a semiconductor device with reduced gate wrap around, comprising:

providing a substrate having a substantially planar surface;

providing a first silicon oxide layer over the substrate;

providing a trench in the substrate through the silicon oxide layer, an intersection of the trench and the surface of the substrate forming a corner;

providing a dielectric layer that fills the trench to a level above the first silicon oxide layer;

providing an anti-reflective coating (ARC) layer conformally over the dielectric layer and the first silicon oxide layer;

providing a photoresist mask over the dielectric layer;

etching an exposed portion of the spacer layer through the photoresist mask to form an ARC spacer aligned with the dielectric layer, the ARC spacer protecting the dielectric layer from loss proximate the corner; and

removing the ARC spacer.

16. The method of Claim 15, wherein the first silicon oxide layer has a thickness between about 150 Å and about 200 Å.

17. The method of Claim 15, wherein the spacer layer comprises propylene glycol monomethyl ether, aromatic sulfur compound, acrylic polymer, non-ionic surfactant, residual acrylate monomer, amidomethyl ether crosslinker, and 2-methoxy-1-propanol.

18. The method of Claim 15, wherein the spacer layer has a thickness between about 700 Å and about 900 Å.

19. The method of Claim 15, wherein the photoresist mask is provided over the first silicon oxide layer.

20. The method of Claim 15, wherein the ARC spacer has a width adjacent the first silicon oxide layer between about 400 Å and about 1,000 Å.

21. The method of Claim 15, further comprising:

etching a portion of the first silicon oxide layer through the photoresist mask and around the ARC spacer;

removing the photoresist mask, a remainder of the spacer layer, and the ARC spacer;

providing a second silicon oxide layer over the substrate; and

providing a polysilicon layer over the dielectric layer, over a remaining portion of the first silicon oxide layer, and over the second silicon oxide layer.

22. The method of Claim 21, wherein the second silicon oxide layer has a thickness between about 50 Å and about 70 Å.

23. The method of Claim 21, wherein the second silicon oxide layer is provided between remaining portions of the first silicon oxide layer.

24. The method of Claim 21, wherein the remaining portions of the first silicon oxide layer have a greater thickness than the second silicon oxide layer.

25. The method of Claim 15, further comprising:

providing a nitride layer over the first silicon oxide layer;

patterning the nitride layer;

forming a trench in the substrate through the patterned nitride layer;

filling the trench with a dielectric layer to a level substantially coplanar with a top surface of the nitride layer; and

removing the nitride layer.

26. A semiconductor device structure, comprising:

a substrate having a substantially planar surface;

a first oxide layer over the surface of the substrate;

a trench in the substrate, an intersection of the trench and the surface of the substrate forming a corner;

a dielectric layer that fills the trench to a level above the first oxide layer; and

a second oxide layer over the substrate between portions of the first oxide layer, the portions of the first oxide layer having a larger thickness than the second oxide layer.

27. The structure of Claim 26, wherein the first oxide layer has a thickness between about 150 Å and about 200 Å.

28. The structure of Claim 26, wherein the second oxide layer has a thickness between about 50 Å and about 70 Å.

29. The structure of Claim 26, wherein the second oxide layer has lower capacitance per unit area than the portions of the first oxide layer.